REMARKS/AMENDMENTS

I. Introductory Remarks.

The Applicant wishes to thank the Examiner for the courtesies extended during the telephone conference call on 11 July 2006 and his comments in the Office Action mailed 13 June 2006. This paper addresses the issues raised in the Office Action and the discussion with the Examiner regarding the non-obviousness of Applicants invention and filing a Request for Continued Examination. Claims 1-20 are currently pending in the application. In the Office Action of 13 June 2006, the Examiner rejected Claims 1-14 and 18-20. Claims 15-17 were withdrawn from consideration. Claims 1-14 and 18-20 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description. Additionally, Claims 1-4, 7-14 and 18-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chino et al. or Miyakuni et al. as evidenced by Demmin. Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chino or Miyakuni, and further in view of Hayasaka et al.

II. Rejection of Claims 1-14 and 18-20 under 35 U.S.C. § 112, first paragraph

Claims 1-14 and 18-20 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. In Claims 1 and 18, "limited to the compound semiconductor material" is considered new matter by the Examiner since Applicant's disclosure, specifically, [0017], line 6, states that the structure comprises a compound semiconductor material. The Examiner refers to the transitional term "comprising" as inclusive or open-ended. Therefore, the Examiner believes that it would have been obvious to one with ordinary skill in the art that the structure is not limited to a compound semiconductor material. Further, the Examiner discusses that any negative limitation must have basis in the original disclosure. Applicant believes that the original disclosure, specifically paragraphs [0017], [0020] and [0022] contains the subject matter in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claims 1 and 18, which are the independent claims, are herein amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicant's belief that the claims would have been allowable as originally filed. Applicant has deleted the "limited to the compound semiconductor material" and added that the compound semiconductor material is selectively etched in the semiconductor material without punch-through of the metal layer. Amended Claim 1 now reads:

> Claim 1 A dry etching process for a semiconductor wafer having variable thickness comprising the steps of:
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> placing in a chamber said semiconductor wafer having on one side a compound semiconductor material with an exposed portion and on the opposing side a metal layer;
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> releasing an halogen etchant into said chamber;
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> adding a nitrogen gas to said chamber;
>
> heating said compound semiconductor material;
>
> applying pressure to said halogen etchant and said nitrogen gas;
>
> applying a bias power and a pulse-modulated power to said halogen etchant and said nitrogen gas; and
>
> continuing the dry etching process until a desired via-hole is selectively etched in the compound semiconductor material to produce vertical sidewalls in X and Y crystalline directions therein without punch-through of the metal layer.

Claim 18, has correspondingly been amended to encompass these embodiments. No new matter has been added. Reconsideration of the present application in light of the foregoing amendment and following remarks is respectfully requested.

II. Rejection of Claims 1-4, 7-14 and 18-20 under 35 U.S.C. §103(a).

Claims 1-4, 7-14 and 18-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chino et al. or Miyakuni et al. as evidenced by Demmin. Claims 1 and

18 have been amended to incorporate the selectivity of the etching process to produce vertical sidewalls in X and Y crystalline directions in a compound semiconductor material having a variable thickness, without metal punch-through. Chino or Miyakuni do not teach the ability to etch vertical sidewalls in a compound semiconductor material that has a large thickness variation across it, nor the ability to prevent punch-through of a metal layer.

The currently amended Claims 1 and 18, encompass a dry etching process that selectively etches the compound semiconductor material to produce vertical sidewalls, regardless of the thickness across the compound semiconductor material, without punch-through of the metal layer. Neither Chino or Miyakuni teach the ability to dry etch a compound semiconductor wafer that has a variable thickness without resulting in punch through to the metal layer in areas where the semiconductor material is thinner. In addition, the processes disclosed in Chino or Miyakuni are not selective enough to prevent punch through of the opposing side metal layer, as evidenced by Chino and Miyakuni each requiring an etching stopper layer to prevent punch through.

An etching stopper layer is not required in Applicant's invention, despite the fact that the compound semiconductor material may have a thickness differential across it. The Applicant's claimed process is selective enough to etch one side of the wafer faster (i.e. the backside having the semiconductor material) than the opposing side (i.e. the front-side having a metal layer), thereby preventing punch-through of the metal layer, even with material thickness variations across the wafer.

The Examiner has taken official notice that it is obvious to one with ordinary skill in the art to etch a via-hole, which is a well-known feature in the semiconductor device fabrication. Applicant respectfully traverses the Examiner's official notice of how to etch a via-hole as applied to the present invention. The Applicant's inventive way of selectively etching a via-hole in a semiconductor material having a variable thickness is not known or common knowledge in the art. Applicant's invention solves the problem of how to etch a via hole when there is a variable thickness without punch through of the metal layer. Without Applicants novel invention, semiconductor wafers having a variable thickness will

likely be rendered inoperable and ruined after the etching process. Applicants invention expertly addresses the problem of no longer ruining wafers by punch through to the metal layer while etching, not the broad concept of a etching a via hole.

The Examiner concedes that the current claims in Applicants invention differ from the prior art by specifying various processing parameters. The rejection based on combining Demmin to show the evidence of the teaching of Chino or Miyakuni, that the same result-effective variables are commonly determined by routine experiment fails because the prior art cited, Chino or Miyakuni, never teach the claimed process. Applicants invention is unobvious in view of Demmin given that the selective etching processes in Claims 1-4, 7-14 and 18-20 are not obvious in Chino or Miyakuni. Therefore, Demmin cannot be used as evidence in combination with Chino or Miyakuni, since Chino and Miyakuni fail to teach Applicants invention. Therefore, the Applicants respectfully request that this ground for rejection on this basis be withdrawn and that Claims 1-4, 7-14 and 18-20 be passed to allowance.

III. Rejection of Claims 5 and 6 under 35 U.S.C. §103(a).

Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chino or Miyakuni as applied to Claims 1 and 3 above, and further in view of Hayasaka et al.

As discussed elsewhere in these remarks, Chino or Miyakuni fail to teach a dry etching process for producing vertical sidewalls in X and Y crystalline directions along a compound semiconductor material having a variable thickness, without punch through to the opposing side metal layer by using halogen etchant in combination with nitrogen gas.

Hayasaka is used to show that it is a well-known feature in the art of semiconductor device fabrication that halogen-containing gas may be used for etching and that the halogen-containing gas can include chlorine, bromine, hydrogen bromide or hydrogen iodide. However, since Chino or Miyakuni fail to teach the Applicants inventive process, combining Hayasaka with the references does not attain the selective etching process as

claimed by Applicant. Without the process being taught by Chino or Miyakuni, the fact that Hayasaka merely discusses use of halogen-containing gas in etching, does not render Applicants invention anymore obvious when combined with Chino or Miyakuni. Therefore, the Applicants respectfully request that this ground for rejection on this basis be withdrawn and that Claim 5 and 6 be passed to allowance.

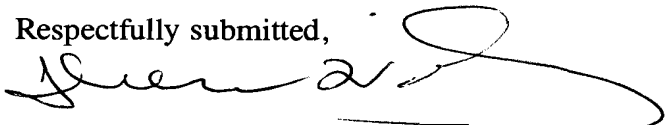
IV. Further Amendment Remarks.

In light of the amendments to Claims 1 and 18, the rejections set forth in the pending Office action are rendered moot, and the Claims, as amended, remaining in this application are in a condition for allowance. Reconsideration of these rejections is respectfully requested. No new matter has been introduced by this amendment.

CONCLUSION

The Applicants would like to thank the Examiner again for the telephone conversation of 11 July 2006 and the remarks in the Office Action dated 13 June 2006. Applicants respectfully request that Claims 1-14 and 18-20 as herein amended to better encompass the full scope and breadth of the present invention be reconsidered in light of the foregoing amendment and remarks, notwithstanding Applicants' belief that the claims would have been allowable as originally filed. Applicant reserves the right to file one or more continuation applications based on the above referenced application. The Examiner is further cordially invited to telephone the undersigned for any reason, which would advance the allowance of the pending claims.

Respectfully submitted,



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